A C-BAND 25 WATT LINEAR POWER FET

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ABSTRACT

A novel four-way power combiner/divider based on 1/8-wavelength transmission line consideration is applied to the design of internally matched GaAs FETs. The resultant FET delivers an output power at 1 dB gain compression point of 44 dBm (25 W) with 12 dB linear gain, 40 % power added efficiency, and -46 dBc 3rd order intermodulation distortion at an output power of 35 dBm (single carrier level), over the 4.4 to 5.0 GHz frequency range.

INTRODUCTION

Recent trends of digital communication systems with multilevel signals require Solid State Power Amplifiers (SSPA's) with higher power, higher gain and lower distortion. In SSPA's of C-band, the 10 W class GaAs FETs with internally matched circuits have traditionally been used [1]. Typically, the internal matching circuits for multi-chips combining consist of 1/4-wavelength power combiner/dividers. At C-band, however, the 1/4-wavelength line are prohivitively large. Circuit size may be reduced by using high dielectric substrates. But these substrates result in relatively narrow transmission lines with high insertion loss. It is very important to reduce the size without the decrease of the line-width. For this purpose, the 1/8-wavelength four-way power combiner/divider was developed. To illustrate its application, a newly developed internally matched GaAs FET based on this combiner/divider is described.

MEASUREMENT OF OPTIMUM IMPEDANCE

In the design of matching networks for linear power FETs, it is important to optimize the network for intermodulation distortion as well as output power and linear gain. Therefore, the load impedance of the matching network must be chosen to simultaneously satisfy requirements of output power at 1 dB gain compression point (P_{1dB}), linear gain (G_L), and 3rd order intermodulation distortion (IM_3). The FET chip used in this application has a total gate width of 18.0 mm and consists of twelve 1.5 mm unit cell FETs connected in parallel. A load-pull based load impedance analysis was performed on the unit cell FET because the impedance of the 18 mm FET is too low to analyze precisely. Figure 1 shows the load impedance contours for constant P_{1dB}, G_L and IM_3 of the unit cell FET at the high band-edge of 5.0 GHz. The shaded region indicates load impedances which simultaneously yield P_{1dB} greater than 28 dBm, G_L greater than 13.5 dB, and IM_3 lower than -48 dBc at an output power of 19 dBm (single carrier level). The matching network optimization has been carried out through full frequency range of 4.4 to 5.0 GHz by the Super Compact. Similar analysis has been done for the input side of the matching network.

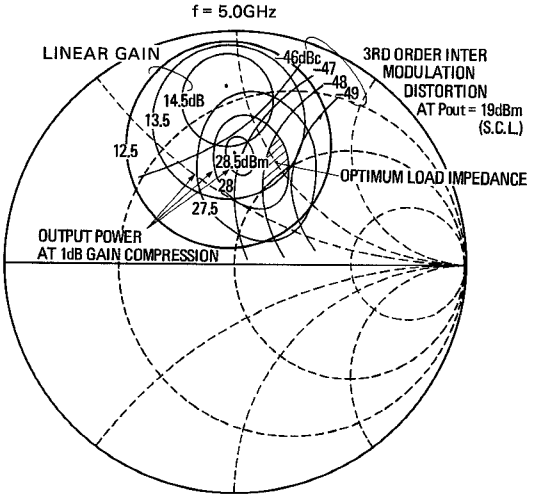

Fig. 1 Load Impedance Contours for Constant P_{1dB}, G_L and IM_3 of Unit FET

From the unit cell load impedance data, an amplifier using the twelve cell 18 mm FET chip was designed and fabricated. The amplifier achieves a P_{1dB} of 38.7 dBm, G_L of 12.8 dB and IM_3 of -47 dBc at an output power of 29 dBm (single carrier level) at 4.7 GHz; therefore, an amplifier combining four of these chips should meet the P_{1dB} goal of 44 dBm. These results confirm that our design approach is effective in the design of matching networks for linear amplifier.

DESIGN OF MATCHING NETWORK

Because the full 18 mm FET is a parallel combination of twelve unit cell FETs, input and output impedances of the FET become less than 1 ohm and a few ohms, respectively. The matching network must provide a high impedance transformation ratio from the impedance of the FET to 50 ohms over the required bandwidth (in this case the fractional bandwidth of 13 %). Usually, a matching network for four-chips combining consists of the two stages of the 1/4-wavelength transmission-line combiner/divider to give a high transformation ratio. At C-band, however, this network with 1/4-wavelength lines has a disadvantage in the size. So, usually, to reduce the size, the high dielectric substrates are used as the substrate for the internally matched circuit. However, the use of the high dielectric substrate results in the decrease of the line-width and in the increase of the insertion-loss. The newly designed four-way power combiner/divider consists of the two stages of two 1/8-wavelength transmission line arms as shown in Figure 2. The characteristic impedances of each stage: Z_1 and Z_2, are expressed by

$$Z_1 = (Z_S \cdot Z_L)^{1/2} \text{ : outer stage}$$
$$Z_2 = 2\,(Z_S \cdot Z_L)^{1/2} \text{ : inner stage}$$

where Z_S is the port impedance of the branch
Z_L is the port impedance of the root

The circuit diagram of the newly designed matching network is shown in figure 3. The matching network consists of the four-way power combiner/divider which is comprised of microstrip lines, and the impedance transformers, which are formed by lumped L-C elements for small size and wide bandwidth. Figure 4 shows the fractional bandwidth as a function of the port impedance ratio (Z_L/Z_S) of this combiner/divider in the case of the VSWR lower than 1.4, which is low enough to use in a 50 ohms circuit. To obtain low VSWR over the required bandwidth, the combiner/divider should have a Z_L/Z_S ratio of less than 3 corresponding to a branch port impedance of 20 to 30 ohms for the root port impedance of 50 ohms. Low VSWR is obtained over full frequency range by optimizing Z_1, Z_2 and the line-length of each stage. Figure 5 shows the fractional bandwidth as a function of the impedance transformation ratio, Z_L/Z_S, for the lumped element input and output impedance transformers in the case of VSWR lower than 1.2. The output transformer consists of a single section formed by lumped L-C elements. It transforms the FET's output impedance of about 5 ohms to the branch port impedance of 20 ohms. This impedance transformation ratio is about 4, which gives the required fractional bandwidth of 13 %. For the input, two sections of lumped L-C elements are used to achieve a higher transformation ratio from the FET's input impedance less than 1 ohm to 30 ohms. The impedance transformation ratio is about 60, which gives wider fractional bandwidth than that required.

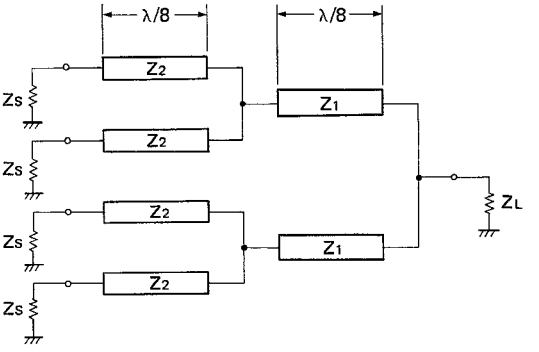

Fig. 2 Newly Designed Four-way Power Combiner/Divider

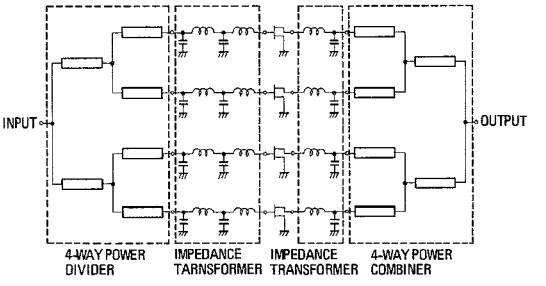

Fig. 3 Circuit Diagram of Newly Designed Matching Network

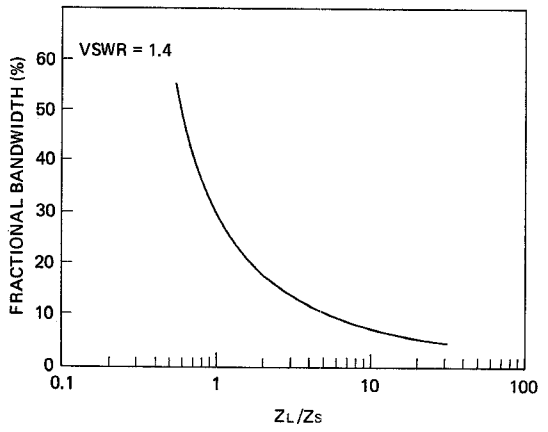

Fig. 4 Fractional Bandwidth as function of Port Impedance Ratio (Z_L/Z_s) of Newly Four-way Combiner/Divider

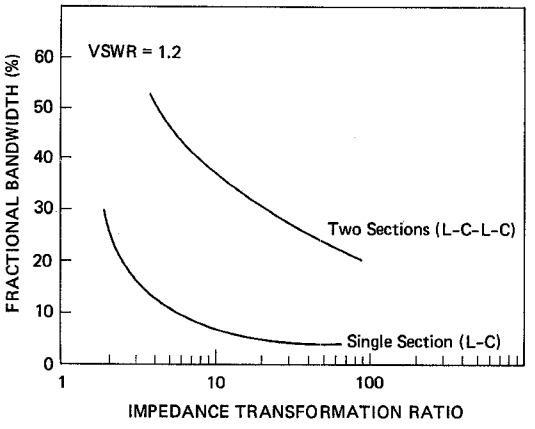

Fig. 5 Fractional Bandwidth as function of Impedance Transformation Ratio of Impedance Transformer

FABRICATION

Figure 6 shows an internal view of the newly developed internally matched GaAs FET. The external package size is 17.4 mm x 24.0 mm. The GaAs FET chip has a total gate width of 18.0 mm to achieve the required output power when four chips are combined. To achieve high gain, reduction of gate length and optimization of unit gate width are generally accepted technique. This FET has a gate length of 0.5μm and unit gate width of 125 μm. The substrates for the 1/8-wavelength combining and dividing circuits are made of alumina and have the thickness of 0.38 mm and dielectric constant of 9.8. The transmission lines on the substrates are sufficiently wide to have low insertion loss and handle the required drain current. The lumped element capacitors are fabricated on a the high dielectric substrate which has the thickness of 0.15 mm and dielectric constant of 140. The electrode of the capacitor is partitioned into two sections so that its width does not exceed 1/4-wavelength. The inductors are implemented with 25 μm diameter gold wires. Eight wires are bonded to satisfy the MIL-STD current capacity specification.

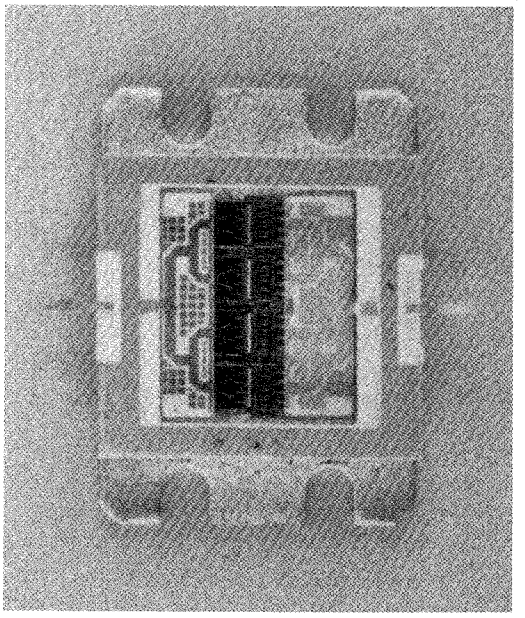

Fig. 6 Inner View of Newly Developed Internally Matched GaAs FET

RF PERFORMANCE

Figure 7 shows the output power and power added efficiency versus input power at a drain voltage of 10 V and frequency of 4.7 GHz. The amplifier achieves the P_{1dB} of 44.3 dBm (26.9 W) with the G_L of 12.3 dB and the power added efficiency (η_{add}) of 40 %. Figure 8 shows the output power and IM_3 versus input power. The IM_3 at an output power of 35 dBm (single carrier level) is -46 dBc, which is sufficient for use in the digital communication systems. Figure 9 shows the frequency response of P_{1dB} and G_L . P_{1dB} flatness less than 0.3 dB and G_L flatness less than 0.5 dB are obtained from 4.4 to 5.0 GHz. The P_{1dB} of the amplifier is only 0.4 dB lower than four times the P1dB of a single FET chip.

This decrease in P_{1dB} includes a power loss contribution of 0.2 dB from a 20 degree-C increase in channel-temperature. The amplifier has a total power combining loss of 0.2 dB (i.e. a power combining efficiency of 95 %). This result shows that the newly developed four-way power combiner/divider is effective in achieving desired performance.

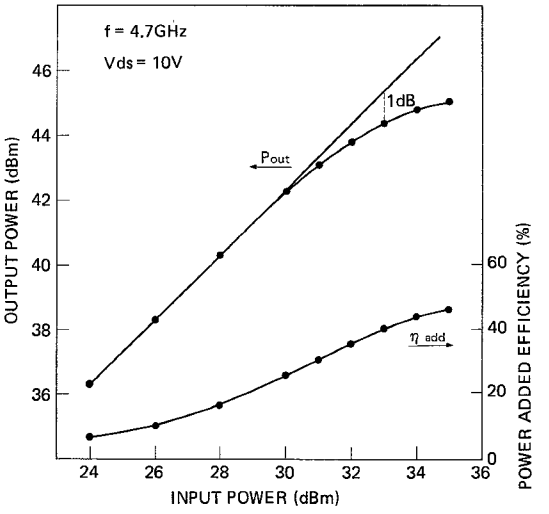

Fig. 7 Output Power and Power Added Efficiency versus Input Power of FET at 4.7 GHz

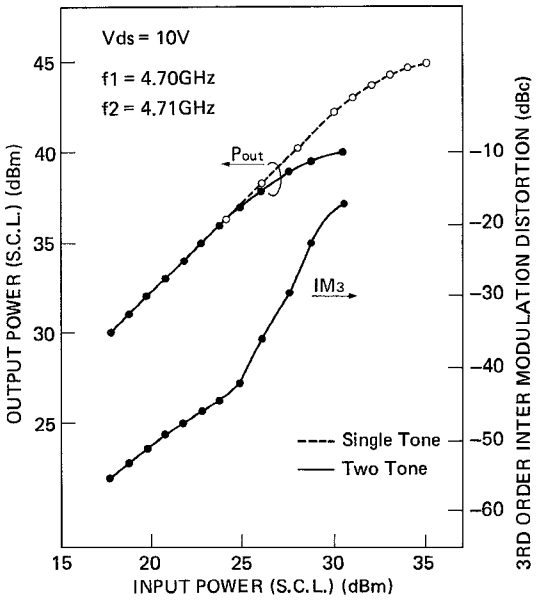

Fig. 8 Output Power (S.C.L.) and IM_3 versus Input Power (S.C.L.) of FET at 4.7 GHz

Note) S.C.L.: Single Carrier Level

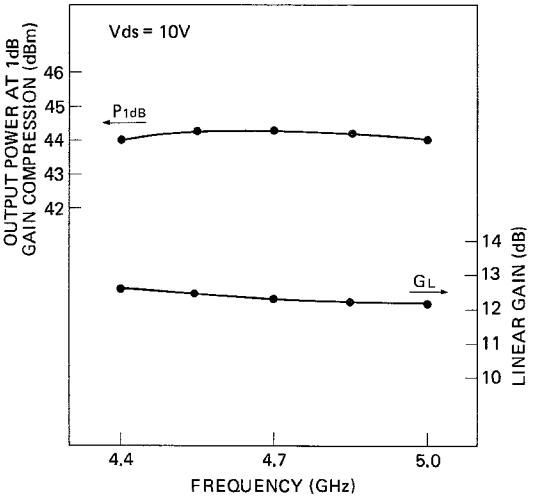

Fig. 9 Frequency Response of P_{1dB} and G_L of FET

CONCLUSION

A C-band 25 watt linear power FET with P_{1dB} of 44.3 dBm, G_L of 12.3 dB, η_{add} of 40 % and IM_3 of -46 dBc has been developed utilizing a novel four-way power combiner/divider. This FET has sufficient performance for use in digital communication systems.

REFERENCE

[1] S.Takase, Y.Hirano, Y.Taniguchi, T.Ohno, and K.Ohta "HIGH GAIN, HIGH POWER ADDED EFFICIENCY GaAs POWER FET FOR SATELLITE USE; ITS DESIGN AND RELIABILITY", 19th EUMC, Sep. 1989.